In the Claims:

1. (Original) A memory cell comprising:

a p-well area having at least one NMOS transistor formed therein, the NMOS transistor having an NMOS active area; and

an n-well area having at least one PMOS transistor formed therein; and

wherein the memory cell has a long side and a short side, the long side being at least twice as long as the short side, a longitudinal axis of the p-well being parallel to the short side.

2. (Original) The memory cell of claim 1, wherein the memory cell is a 6T-SRAM cell.

3. (Original) The memory cell of claim 2, wherein maximum resistance between cells p-well to p-well strap contact is less than 4000 ohm.

4. (Original) The memory cell of claim 2, wherein maximum distance between cells p-well to p-well low resistance strap is less than 3.6 μm.

5. (Original) The memory cell of claim 2, wherein the p-well area is less than about 65% of the memory cell.

6. (Original) The memory cell of claim 2, wherein the distance from the n-well area to the NMOS active area is less than about 75 nm.

7. (Original) The memory cell of claim 2, wherein the NMOS active region is less than about 25% of the memory cell.

8. (Original) The memory cell of claim 2, wherein the short side is less than about 0.485 μm.

9. (Original) The memory cell of claim 1, wherein the memory cell is an 8T-SRAM cell.

10. (Original) The memory cell of claim 9, wherein maximum resistance between cells p-well to p-well strap contact is less than 4000 ohm.

11. (Original) The memory cell of claim 9, wherein maximum distance between cells p-well to p-well low resistance strap is less than 3.6 μm.

12. (Original) The memory cell of claim 9, wherein the p-well area is less than about 75% of the memory cell.

13. (Original) The memory cell of claim 9, wherein the distance from the n-well area to the NMOS active area is less than about 100 nm.

14. (Original) The memory cell of claim 9, wherein the NMOS active region is less than about 33% of the memory cell.

15. (Original) The memory cell of claim 9, wherein the short side is less than about 0.745 μm.

16. (Original) The memory cell of claim 1, wherein the n-well is a deep n-well.

17. (Original) The memory cell of claim 1, wherein the p-well substantially encircles the n-well.

18. (Original) The memory cell of claim 1, wherein the memory cell includes a plurality of V_{ss} lines, the plurality of V_{ss} lines being located on one or more metal layers.

19. (Original) The memory cell of claim 1, wherein the memory cell has an area of less than about 0.4 μm2, at least one of the PMOS transistors or the NMOS transistors have a gate thickness less than about 1000 Å.

20. (Original) The memory cell of claim 1, wherein the NMOS transistor has a gate layer and a gate dielectric layer and the gate dielectric layer having one or more layers and at least one layer comprising SiO2, nitrided oxide, nitrogen content oxide, SiON, metal oxide, high K dielectric, or a combination thereof.

21. (Original) The memory cell of claim 1, wherein the memory cell includes at least one pull-down transistor having a gate width of less than about 40 nm and a gate dielectric thickness of less than 13 Å.

22. (Original) The memory cell of claim 1, wherein the memory cell has a maximum storage capacitance of less than about 0.5 femto-farad.

23. (Original) The memory cell of claim 1, wherein the memory cell includes at least one bit line, each bit line being parallel to the longitudinal axis of the p-well.

24. (Original) The memory cell of claim 1, wherein the memory cell is formed on a substrate comprising bulk-Si, SiGe, strain-Si, SOI, non-bulk Si, or a combination thereof.

25. (Original) The memory cell of claim 1, wherein the memory cell includes at least one bit line, each bit line having at least one of a V_{cc} line or a V_{ss} line thereof adjacent the bit line.

26. (Original) The memory cell of claim 1, wherein the memory cell includes a plurality of metal layers, and the memory cell includes a bit line and a complementary bit line, the bit line and the complementary bit line being on different metal layers.

27. (Currently Amended) A memory cell comprising:

a p-well area having a first portion and a second portion, the first portion having a first pass-gate transistor and a first pull-down transistor, the second portion having a second pass-gate transistor and a second pull-down transistor; and

an n-well area positioned between the first portion and the second portion, the n-well area having a first pull-up transistor and a second pull-up transistor;

wherein

the memory cell has a long side and a short side, the long side being at least twice as long as the short side, the short side being less than 0.485 μm, and a longitudinal axis of the p-well being parallel to the short ~~side~~ side;

the gate of the first pass-gate transistor is electrically coupled to a word line;

the source of the first pass-gate transistor is electrically coupled to a bit line;

the drain of the first pass-gate transistor is electrically coupled to the drain of the first pull-down transistor;

the source of the first pull-down transistor is electrically coupled to a V_{ss}

line;

the drain of the first pass-gate transistor, the drain of the first pull-up transistor, the drain of the first pull-down transistor, the gate of the second pull-down transistor, and second pull-up transistor are electrically coupled;

the drain of the second pass-gate transistor, the drain of the second pull-up transistor, the drain of the second pull-down transistor, the gate of the first pull-down transistor, and first pull-up transistor are electrically coupled;

the source of the first pull-up transistor is electrically coupled to a V_{cc} line;

the source of the second pull-up transistor is electrically coupled to the V_{cc} line;

the gate of the second pass-gate transistor is electrically coupled to the word line;

the source of the second pass-gate transistor is electrically coupled to a bit line bar;

the drain of the second pass-gate transistor is electrically coupled to the drain of the second pull-down transistor;

the source of the second pull-down transistor is electrically coupled to the V_{ss} line; and

a longitudinal axis along the source-to-direction of each transistor is substantially parallel to the shorter side of the memory cell.

~~a first axis along the source-to-drain direction of the first pass-gate transistor is substantially parallel to the shorter side of the memory cell;~~

~~a second axis along the source-to-drain direction of the first pull-down~~

~~transistor is substantially parallel to the shorter side of the memory cell;~~

~~a third axis along the source-to-drain direction of the first pull-up transistor is substantially parallel to the shorter side of the memory cell;~~

~~a fourth axis along the source-to-drain direction of the second pass-gate transistor is substantially parallel to the shorter side of the memory cell;~~

~~a fifth axis along the source-to-drain direction of the second pull-down transistor is substantially parallel to the shorter side of the memory cell; and~~

~~a sixth axis along the source-to-drain direction of the second pull-up transistor is substantially parallel to the shorter side of the memory cell.~~

28. (Original) The memory cell of claim 27, wherein resistance between a p-well to a p-well strap contact is less than about 4000 ohm.

29. (Original) The memory cell of claim 27, wherein the distance from a p-well to a p-well strap contact is less than about 3.6 um.

30. (Original) The memory cell of claim 27, wherein the p-well area is less than about 65% of the memory cell.

31. (Original) The memory cell of claim 27, wherein the distance of the n-well area to the NMOS active area is less than about 75 nm.

32. (Original) The memory cell of claim 27, wherein the NMOS active region is less than about 25% of the memory cell.

33. (Original) The memory cell of claim 27, wherein the n-well is a deep n-well.

34. (Original) The memory cell of claim 27, wherein the p-well substantially encircles the n-well.

35. (Original) The memory cell of claim 27, wherein the memory cell includes a plurality of V_{ss} lines, the plurality of V_{ss} lines being located on one or more metal layers.

36. (Original) The memory cell of claim 27, wherein the memory cell has an area of less than about 0.4 μm2, at least one of the PMOS transistors or the NMOS transistors have a gate thickness less than about 1000 Å, and the memory cell includes at least one pull-down transistor having a gate width of less than about 40 nm.

37. (Original) The memory cell of claim 27, wherein at least one of the first pull-up transistors and the second pull-up transistor has a gate layer and a gate oxide layer and the gate oxide layer having one or more layers and at least one layer comprising SiO2, nitrided oxide, nitrogen content oxide, SiON, metal oxide, high K dielectric, or a combination thereof.

38. (Original) The memory cell of claim 27, wherein at least one of the first pull-down transistor and the second pull-down transistor have a gate width of less than about 40 nm and a gate oxide thickness of less than 13 Å.

39. (Original) The memory cell of claim 27, wherein the memory cell has a maximum storage capacitance of less than about 0.5 femto-farad.

40. (Original) The memory cell of claim 27, wherein each bit line is parallel to the longitudinal axis of the p-well.

41. (Original) The memory cell of claim 27, wherein the memory cell is formed on a substrate comprising bulk-Si, SiGe, strain-Si, SOI, non-bulk Si, or a combination thereof.

42. (Original) The memory cell of claim 27, wherein the memory cell includes at least one bit line, each bit line having a V_{cc} line and a V_{ss} line adjacent the bit line.

43. (Original) The memory cell of claim 27, wherein the memory cell includes a plurality of metal layers, and the memory cell includes a bit line and a complementary bit line, the bit line and the complementary bit line being on different metal layers.

44. (Currently Amended) A memory cell comprising:

a p-well area having a first portion and a second portion, the first portion having a first pass-gate transistor, a second pass-gate transistor, and a first pull-down transistor, the second portion having a third pass-gate transistor, a fourth pass-gate transistor and a second pull-down transistor; and

an n-well area positioned between the first portion and the second portion, the n-well area having a first pull-up transistor and a second pull-up transistor;

wherein

the memory cell has a long side and a short side, the long side being at least twice as long as the short side, the short side being less than 0.745 μm, and a longitudinal axis of the p-well being parallel to the short ~~side~~ side;

the gates of the first pass-gate transistor and second pass-gate transistor are electrically coupled to a first word line;

the gates of the third pass-gate transistor and fourth pass-gate transistor are electrically coupled to a second word line;

the source of the first pass-gate transistor is electrically coupled to a first bit line;

the source of the third pass-gate transistor is electrically coupled to a second bit line;

the drain of the first pass-gate transistor is electrically coupled to the drain of the first pull-down transistor;

the source of the first pull-down transistor is electrically coupled to a V_{ss} line;

the source of the second pull-down transistor is electrically coupled to a V_{ss} line;

the drain of the first pass-gate transistor, the drain of the first pull-down transistor, the drain of the first pull-up transistor, the gate of the second pull-down transistor, the gate of the second pull-up transistor, and the drain of the third pass-gate transistor are electrically coupled;

the drain of the fourth pass-gate transistor, the drain of the second pull-down transistor, the drain of the second pull-up transistor, the gate of the first pull-down transistor, the gate of the first pull-up transistor, and the drain of the second pass-gate transistor are electrically coupled;

the source of the first pull-up transistor is electrically coupled to a V_{cc} line;

the source of the second pull-up transistor is electrically coupled to the V_{cc} line;

the source of the second pass-gate transistor is electrically coupled to a first complementary bit line;

the source of the fourth pass-gate transistor is electrically coupled to a second complementary bit line; and

a longitudinal axis along the source-to-direction of each transistor is substantially parallel to the shorter side of the memory cell.

~~a first axis along the source to drain direction of the first pass gate transistor is substantially parallel to the shorter side of the memory cell;~~

~~a second axis along the source to drain direction of the first pull down transistor is substantially parallel to the shorter side of the memory cell;~~

~~a third axis along the source to drain direction of the first pull up transistor is substantially parallel to the shorter side of the memory cell;~~

~~a fourth axis along the source to drain direction of the second pass gate transistor is substantially parallel to the shorter side of the memory cell;~~

~~a fifth axis along the source to drain direction of the second pull down transistor is substantially parallel to the shorter side of the memory cell;~~

~~a sixth axis along the source to drain direction of the second pull up transistor is substantially parallel to the shorter side of the memory cell;~~

~~a seventh axis along the source to drain direction of the third pass gate transistor is substantially parallel to the shorter side of the memory cell; and~~

~~an eigth axis along the source to drain direction of the fourth pass gate transistor is substantially parallel to the shorter side of the memory cell.~~

45. (Original) The memory cell of claim 44, wherein resistance between a p-well to a p-well strap contact is less than about 4000 ohm.

46. (Original) The memory cell of claim 44, wherein the distance from a p-well to a p-well strap contact is less than about 3.6um.

47. (Original) The memory cell of claim 44, wherein the p-well area is less than about 75% of the memory cell.

48. (Original) The memory cell of claim 44, wherein the distance of the n-well area to the NMOS active area is less than about 100 nm.

49. (Original) The memory cell of claim 44, wherein the NMOS active region is less than about 33% of the memory cell.

50. (Original) The memory cell of claim 44, wherein the n-well is a deep n-well.

51. (Original) The memory cell of claim 44, wherein the p-well substantially encircles the n-well.

52. (Original) The memory cell of claim 44, wherein the memory cell includes a plurality of V_{ss} lines, the plurality of V_{ss} lines being located on one or more metal layers.

53. (Original) The memory cell of claim 44, wherein the memory cell has an area of less than about 1.2 μm2, at least one of the PMOS transistors or the NMOS transistors, have a gate thickness less than about 1000 Å.

54. (Original) The memory cell of claim 44, wherein at least one of the first pull-up transistors and the second pull-up transistor has a gate layer and a gate oxide layer and the gate oxide layer having one or more layers and at least one layer comprising SiO2,

nitrided oxide, nitrogen content oxide, SiON, metal oxide, high K dielectric, or a combination thereof.

55. (Original) The memory cell of claim 44, wherein at least one of the first pull-down transistor and the second pull-down transistor have a gate width of less than about 40 nm and a gate oxide thickness of less than 13 Å.

56. (Original) The memory cell of claim 44, wherein the memory cell has a maximum storage capacitance of less than about 1 femto-farad.

57. (Original) The memory cell of claim 44, wherein each bit line is parallel to the longitudinal axis of the p-well.

58. (Original) The memory cell of claim 44, wherein the memory cell is formed on a substrate comprising bulk-Si, SiGe, strain-Si, SOI, non-bulk Si, or a combination thereof.

59. (Original) The memory cell of claim 44, wherein the memory cell includes at least one bit line, each bit line having at least on of a V_{cc} line or a V_{ss} line adjacent the bit line.

60. (Currently Amended) A method of forming a memory cell, the method comprising the steps of:

providing a p-type substrate having a p-well;

forming an n-well in the p-type substrate;

forming in the n-well a first pull-up transistor and a second pull-up transistor; and

forming in the p-well a first pass-gate transistor, a second pass-gate transistor, a first pull-down transistor, and a second pull-down transistor;

wherein the memory cell has a shorter side and a longer side, the longer side being at least twice as long as the shorter side, and wherein the source-to-drain axis of each transistor is parallel to the shorter side.

61. (Original) The method of 60, wherein the n-well is less than about 65% of the memory cell.

62. (Original) The method of 60, wherein maximum distance between any p-well location to a p-well low resistance strap is less than about 3.6 μm.

63. (Original) The method of 60, wherein the distance between an NMOS active area and the n-well is less than about 75 nm.

64. (Original) The method of 60, wherein the shorter side is less than about 0.485 μm.

65. (Original) The method of 60, wherein the n-well is a deep n-well.

66. (Currently Amended) A method of forming a memory cell, the method comprising the steps of:

providing a p-type substrate having a p-well;

forming an n-well in the p-type substrate;

forming in the n-well a first pull-up transistor and a second pull-up transistor; and

forming in the p-well a first pass-gate transistor, a second pass-gate transistor, a third pass-gate transistor, a fourth pass-gate transistor, a first pull-down transistor, and a second pull-down transistor;

wherein the memory cell has a shorter side and a longer side, the longer side

being at least twice as long as the shorter side, and wherein the source-to-drain axis of each transistor is parallel to the shorter side.

67. (Currently Amended) The method ~~of 65~~ of 66, wherein the n-well is less than about 75% of the memory cell.

68. (Currently Amended) The method ~~of 65~~ of 66, wherein maximum distance between any p-well location to a p-well low resistance strap is less than about 3.6 μm.

69. (Currently Amended) The method ~~of 65~~ of 66, wherein the distance between an NMOS active area and the n-well is less than about 100 nm.

70. (Currently Amended) The method ~~of 65~~ of 66, wherein the shorter side is less than about 0.745 μm.

71. (Currently Amended) The method ~~of 65~~ of 66, wherein the n-well is a deep n-well.